



# 82540EP Gigabit Ethernet Controller

*Networking Silicon*

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**Datasheet**

## Product Features

- PCI Bus
  - PCI Revision 2.3 support for 32-bit wide interface at 33 MHz and 66 MHz
  - Algorithms that optimally use advanced PCI, MWI, MRM, and MRL commands
  - CardBus Information Services (CIS) Pointer
  - CLK\_RUN# Signal
- MAC Specific
  - Low-latency transmit and receive queues
  - IEEE 802.3x-compliant flow-control support with software-controllable thresholds
  - Caches up to 64 packet descriptors in a single burst
  - Programmable host memory receive buffers (256 B to 16 KB) and cache line size (16 B to 256 B)
  - Wide, optimized internal data path architecture
  - 64 KB configurable Transmit and Receive FIFO buffers
- PHY Specific
  - Integrated for 10/100/1000 Mb/s operation
  - IEEE 802.3ab Auto-Negotiation support
  - IEEE 802.3ab PHY compliance and compatibility. State-of-the-art DSP architecture implements digital adaptive equalization, echo cancellation, and cross-talk cancellation
  - Automatic detection of cable lengths and MDI vs. MDI-X cable at all speeds
- Host Off-Loading
  - Transmit and receive IP, TCP, and UDP checksum off-loading capabilities
  - Transmit TCP segmentation
  - Advanced packed filtering
  - Jumbo frame support up to 16 KB
  - IEEE 802.1q VLAN support with VLAN tag insertion, stripping and packet filtering for up to 4096 VLAN tags
  - Descriptor ring management hardware for transmit and receive
  - Interrupt coalescing (multiple packets per interrupt)
- Manageability
  - Manageability features: Onboard SMB port, ASF 1.0, ACPI, Wake on LAN, and PXE
  - Compliance with PCI Power Management 1.1 and ACPI 2.0 register set compliant
  - SNMP and RMON statistic counters
  - SDG 3.0, WfM 2.0, and PC2001 compliance
- Additional Device
  - Four activity and link indication outputs that directly drive LEDs
  - JTAG (IEEE 1149.1) Test Access Port built in silicon
  - Internal PLL for clock generation can use a 25 MHz crystal
  - Programmable LED functionality
  - Industrial temperature support (-40 to +85 °C)



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# Revision History

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| Date      | Revision | Notes                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Apr 2002  | 0.25     | Initial Release                                                                                                                                                                                                                                                                                                                                                                                                                 |
| Nov 2002  | 1.0      | Changed document status to Intel Confidential.                                                                                                                                                                                                                                                                                                                                                                                  |
| Jan 2003  | 1.1      | Section 1.0. Replaced Block Diagram<br>Section 2.6. Added Table footnote<br>Section 4.1, 4.2, 4.3. Replaced tables<br>Section 5.1. Added Visual Pin Reference<br>Section 4.4 Removed Power Supply Characteristics; added note to I/O Characteristics<br>Section 5.0 Replaced Pinout Diagram                                                                                                                                     |
| Apr 2003  | 1.2      | Removed confidential status.<br>Section 1.0. Added product ordering code.                                                                                                                                                                                                                                                                                                                                                       |
| Oct 2003  | 1.3      | Updated Table 8 to reflect correct values for internal pull-up impedance.                                                                                                                                                                                                                                                                                                                                                       |
| Nov 2004  | 1.4      | Added product features to cover.<br>Updated signal names to match design guide and reference schematics.                                                                                                                                                                                                                                                                                                                        |
| Nov 2004  | 1.5      | Added information about migrating from a 2-layer 0.36 mm wide-trace substrate to a 2-layer 0.32 mm wide-trace substrate. Refer to the section on Package and Pinout Information.<br>Added statement that no changes to existing soldering processes are needed for the 2-layer 0.32 mm wide-trace substrate change in the section describing "Package Information".<br>Corrected pinout discrepancies between Tables 35 and 36. |
| July 2006 | 1.6      | Added LAN-disable description to the FLSH_SO signal description in Section 3.                                                                                                                                                                                                                                                                                                                                                   |
| Sept 2006 | 1.7      | Added industrial temperature values to "Product Features" and Table 2.<br>Added a note to Figure 12 clarifying the device pin 1 location.                                                                                                                                                                                                                                                                                       |



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## 1.0 Introduction

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The Intel® 82540EP Gigabit Ethernet Controller is a single, compact component with an integrated Gigabit Ethernet Media Access Control (MAC) and physical layer (PHY) functions. For desktop, workstation and mobile PC Network designs with critical space constraints, the Intel® 82540EP allows for a Gigabit Ethernet implementation in a very small area that is footprint compatible with current generation 10/100 Mbps Fast Ethernet designs

The Intel® 82540EP integrates Intel's fourth generation gigabit MAC design with fully integrated, physical layer circuitry to provide a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). The controller is capable of transmitting and receiving data at rates of 1000 Mbps, 100 Mbps, or 10 Mbps. In addition to managing MAC and PHY layer functions, the controller provides a 32-bit wide direct Peripheral Component Interconnect (PCI) 2.2 compliant interface capable of operating at 33 or 66 MHz.

The 82540EP also incorporates the CLK\_RUN# protocol and hardware supported downshift capability to two or three-pair 100 Mb/s operation. These features optimize mobile applications.

The Intel® 82540EP's on-board System Management Bus (SMB) port enables network manageability implementations required by information technology personnel for remote control and alerting via the LAN. With SMB, management packets can be routed to or from a management processor. The SMB port enables industry standards, such as Intelligent Platform Management Interface (IPMI) and Alert Standard Forum (ASF), to be implemented using the 82540EP. In addition, on chip ASF 1.0 circuitry provides alerting and remote control capabilities with standardized interfaces.

The 82540EP Gigabit Ethernet Controller architecture is designed to deliver high performance and PCI bus efficiency. Wide internal data paths eliminate performance bottlenecks by efficiently handling large address and data words. The 82540EP controller includes advanced interrupt handling features to limit PCI bus traffic and a PCI interface that maximizes the use of bursts for efficient bus usage. The 82540EP caches up to 64 packet descriptors in a single burst for efficient PCI bandwidth use. A large 64 KByte on-chip packet buffer maintains superior performance as available PCI bandwidth changes. In addition, using hardware acceleration, the controller offloads tasks from the host controller, such as TCP/UDP/IP checksum calculations and TCP segmentation.

The 82540EP is packaged in a 15 mm<sup>2</sup> 196-ball grid array and is pin compatible with both the 82551QM 10/100 Mbps Fast Ethernet Multifunction PCI/CardBus Controller and the 82540EM Gigabit Ethernet Controller (which does not have added power saving features like CLK\_RUN#).

### 1.1 Document Scope

This document contains datasheet specifications for the 82540EP Gigabit Ethernet Controller, including signal descriptions, DC and AC parameters, packaging data, and pinout information.

## 1.2 Reference Documents

This application assumes that the designer is acquainted with high-speed design and board layout techniques. The following documents provide additional information:

- 82544EI/82544GC Gigabit Ethernet Controller Software Developer's Manual, Revision 0.25, Intel Corporation.
- PCI Local Bus Specification, Revision 2.3, PCI Special Interest Group.
- PCI Bus Power Management Interface Specification, Rev. 1.1, PCI Special Interest Group.
- IEEE Standard 802.3, 1996 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3u, 1995 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3x, 1997 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3z, 1998 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- IEEE Standard 802.3ab, 1999 Edition, Institute of Electrical and Electronics Engineers (IEEE).
- Intel Ethernet Controllers Timing Device Selection Guide, AP-419, Intel Corporation.
- PCI Mobile Design Guide, Rev. 1.1, PCI Special Interest Group
- 82540EP/82541(PI/GI/EI) & 82562EZ(EX) Dual Footprint Design Guide, AP-444. Intel Corporation.



### 1.3 Block Diagram

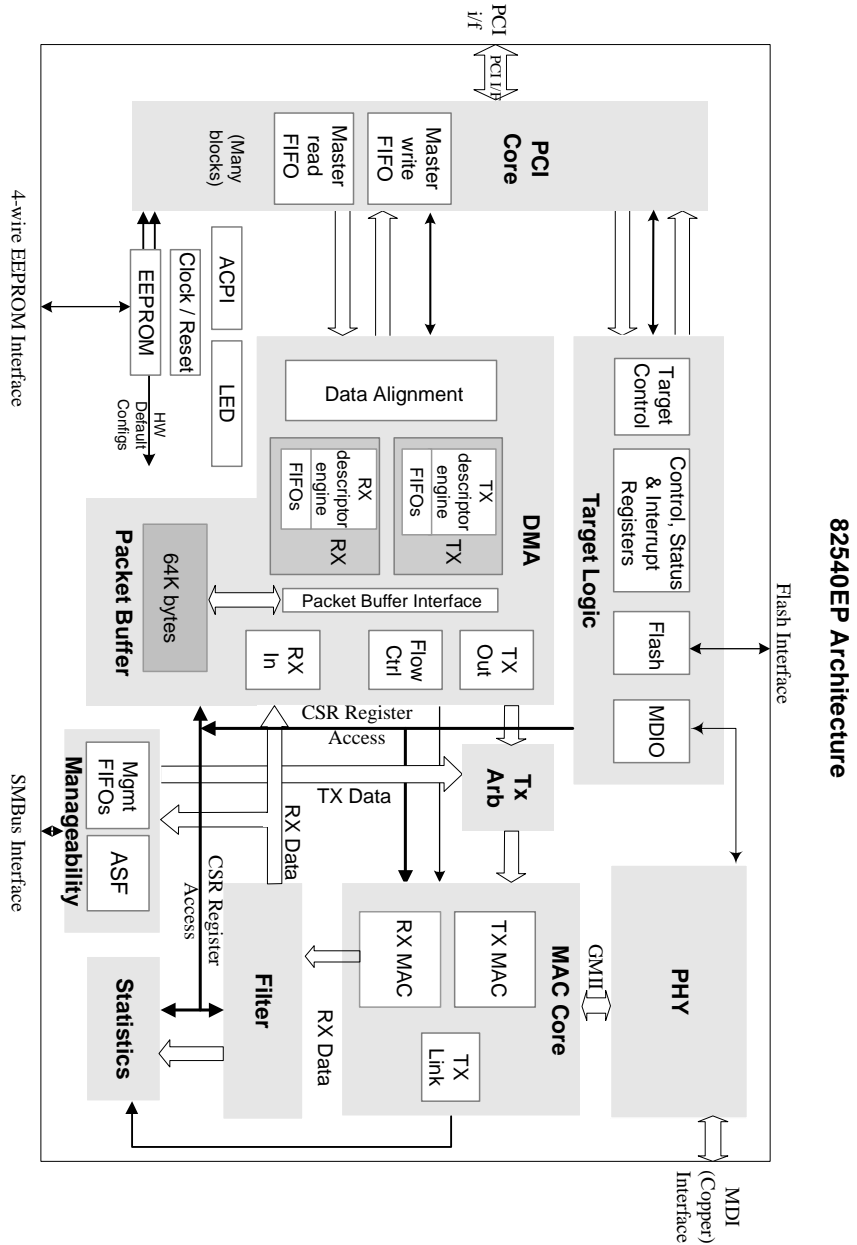


Figure 1. Gigabit Ethernet Controller Block Diagram



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## **2.0 Product Code**

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The product ordering code for the 82540EP is: RC82540EP.



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## 3.0 Signal Descriptions

**Note:** The targeted signal names are subject to change without notice. Verify with your local Intel sales office that you have the latest information before finalizing a design.

### 3.1 Signal Type Definitions

The signals of the 82540EP controller are electrically defined as follows:

| Name | Definition                                                                                                                                                                                                                                                                                                                              |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I    | <b>Input.</b> Standard input only digital signal.                                                                                                                                                                                                                                                                                       |
| O    | <b>Output.</b> Standard output only digital signal.                                                                                                                                                                                                                                                                                     |
| TS   | <b>Tri-state.</b> Bi-directional three-state digital input/output signal.                                                                                                                                                                                                                                                               |
| STS  | <b>Sustained Tri-state.</b> Sustained digital three-state signal driven by one agent at a time. An agent driving the STS pin low must actively drive it high for at least one clock before letting it float. The next agent of the signal cannot drive the pin earlier than one clock after it has been released by the previous agent. |
| OD   | <b>Open Drain.</b> Wired-OR with other agents. The signaling agent asserts the OD signal, but the signal is returned to the inactive state by a weak pull-up resistor. The pull-up resistor may require two or three clock periods to fully restore the signal to the de-asserted state.                                                |
| A    | <b>Analog.</b> PHY analog data signal.                                                                                                                                                                                                                                                                                                  |
| P    | <b>Power.</b> Power connection, voltage reference, or other reference connection.                                                                                                                                                                                                                                                       |

### 3.2 PCI Bus Interface

When the Reset signal (RST#) is asserted, the 82540EP will not drive any PCI output or bi-directional pins except the Power Management Event signal (PME#).

#### 3.2.1 PCI Address, Data and Control Signals

| Symbol   | Type | Name and Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|----------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AD[31:0] | TS   | <p><b>Address and Data.</b> Address and data signals are multiplexed on the same PCI pins. A bus transaction includes an address phase followed by one or more data phases.</p> <p>The address phase is the clock cycle when the Frame signal (FRAME#) is asserted low. During the address phase AD[31:0] contain a physical address (32 bits). For I/O, this is a byte address, and for configuration and memory, a DWORD address. The 82540EP device uses little endian byte ordering.</p> <p>During data phases, AD[7:0] contain the least significant byte (LSB) and AD[31:24] contain the most significant byte (MSB).</p> |

| Symbol     | Type | Name and Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C/BE#[3:0] | TS   | <p><b>Bus Command and Byte Enables.</b> Bus command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE#[3:0] define the bus command. In the data phase, C/BE#[3:0] are used as byte enables. The byte enables are valid for the entire data phase and determine which byte lanes contain meaningful data.</p> <p>C/BE#[0] applies to byte 0 (LSB) and C/BE#[3] applies to byte 3 (MSB).</p>                                                                                                                                                                                                                           |
| PAR        | TS   | <p><b>Parity.</b> The Parity signal is issued to implement even parity across AD[31:0] and C/BE#[3:0]. PAR is stable and valid one clock after the address phase. During data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted after a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase.</p> <p>When the 82540EP controller is a bus master, it drives PAR for address and write data phases, and as a slave device, drives PAR for read data phases.</p>                                                                                |
| FRAME#     | STS  | <p><b>Cycle Frame.</b> The Frame signal is driven by the 82540EP device to indicate the beginning and length of an access and indicate the beginning of a bus transaction. While FRAME# is asserted, data transfers continue. FRAME# is de-asserted when the transaction is in the final data phase.</p>                                                                                                                                                                                                                                                                                                                                                                         |
| IRDY#      | STS  | <p><b>Initiator Ready.</b> Initiator Ready indicates the ability of the 82540EP controller (as bus master device) to complete the current data phase of the transaction. IRDY# is used in conjunction with the Target Ready signal (TRDY#). The data phase is completed on any clock when both IRDY# and TRDY# are asserted.</p> <p>During the write cycle, IRDY# indicates that valid data is present on AD[31:0]. For a read cycle, it indicates the master is ready to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. The 82540EP controller drives IRDY# when acting as a master and samples it when acting as a slave.</p>         |
| TRDY#      | STS  | <p><b>Target Ready.</b> The Target Ready signal indicates the ability of the 82540EP controller (as a selected device) to complete the current data phase of the transaction. TRDY# is used in conjunction with the Initiator Ready signal (IRDY#). A data phase is completed on any clock when both TRDY# and IRDY# are sampled asserted.</p> <p>During a read cycle, TRDY# indicates that valid data is present on AD[31:0]. For a write cycle, it indicates the target is ready to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. The 82540EP device drives TRDY# when acting as a slave and samples it when acting as a master.</p> |
| STOP#      | STS  | <p><b>Stop.</b> The Stop signal indicates the current target is requesting the master to stop the current transaction. As a slave, the 82540EP controller drives STOP# to request the bus master to stop the transaction. As a master, the 82540EP controller receives STOP# from the slave to stop the current transaction.</p>                                                                                                                                                                                                                                                                                                                                                 |
| IDSEL#     | I    | <p><b>Initialization Device Select.</b> The Initialization Device Select signal is used by the 82540EP as a chip select signal during configuration read and write transactions.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| DEVSEL#    | STS  | <p><b>Device Select.</b> When the Device Select signal is actively driven by the 82540EP, it signals notifies the bus master that it has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.</p>                                                                                                                                                                                                                                                                                                                                                                                            |
| VIO        | P    | <p><b>VIO.</b> The VIO signal is a voltage reference for the PCI interface (3.3 V or 5 V PCI signaling environment). It is used as the clamping voltage.</p> <p>Note: An external resistor is required between the voltage reference and the VIO pin. The target resistor value is 100 K <math>\Omega</math>.</p>                                                                                                                                                                                                                                                                                                                                                                |

### 3.2.2 Arbitration Signals

| Symbol | Type | Name and Function                                                                                                                                                                                           |
|--------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REQ#   | TS   | <b>Request Bus.</b> The Request Bus signal is used to request control of the bus from the arbiter. This signal is point-to-point.                                                                           |
| GNT#   | I    | <b>Grant Bus.</b> The Grant Bus signal notifies the 82540EP that bus access has been granted. This is a point-to-point signal.                                                                              |
| LOCK#  | I    | <b>Lock Bus.</b> The Lock Bus signal is asserted by an initiator to require sole access to a target memory device during two or more separate transfers. The 82540EP device does not implement bus locking. |

### 3.2.3 Interrupt Signal

| Symbol | Type | Name and Function                                                                                                                                |
|--------|------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| INTA#  | TS   | <b>Interrupt A.</b> Interrupt A is used to request an interrupt by port 1 of the 82540EP. It is an active low, level-triggered interrupt signal. |

### 3.2.4 System Signals

| Symbol   | Type      | Name and Function                                                                                                                                                                                                                                                                                                                                     |
|----------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLK      | I         | <b>PCI Clock.</b> The PCI Clock signal provides timing for all transactions on the PCI bus and is an input to the 82540EP device. All other PCI signals, except the Interrupt A (INTA#) and PCI Reset signal (RST#), are sampled on the rising edge of CLK. All other timing parameters are defined with respect to this edge.                        |
| M66EN    | I         | <b>66 MHz Enable.</b> M66EN indicates whether the system bus is enabled for 66 MHz.                                                                                                                                                                                                                                                                   |
| RST#     | I         | <b>PCI Reset.</b> When the PCI Reset signal is asserted, all PCI output signals, except the Power Management Event signal (PME#), are floated and all input signals are ignored. The PME# context is preserved, depending on power management settings. Most of the internal state of the 82540EP is reset on the de-assertion (rising edge) of RST#. |
| CLK_RUN# | I/O<br>OD | <b>Clock Run.</b> This signal is used by the system to pause the PCI clock signal. It is used by the 82540EP controller to request the PCI clock. When the CLK_RUN# feature is disabled, leave this pin unconnected.                                                                                                                                  |

### 3.2.5 Error Reporting Signals

| Symbol | Type | Name and Function                                                                                                                                                                                                                                                                                                                                                                                         |
|--------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SERR#  | OD   | <b>System Error.</b> The System Error signal is used by the 82540EP controller to report address parity errors. SERR# is open drain and is actively driven for a single PCI clock when reporting the error.                                                                                                                                                                                               |
| PERR#  | STS  | <b>Parity Error.</b> The Parity Error signal is used by the 82540EP controller to report data parity errors during all PCI transactions except by a Special Cycle. PERR# is sustained tri-state and must be driven active by the 82540EP controller two data clocks after a data parity error is detected. The minimum duration of PERR# is one clock for each data phase a data parity error is present. |

### 3.2.6 Power Management Signals

| Symbol       | Type | Name and Function                                                                                                                                                                                                                                                                       |
|--------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LAN_PWR_GOOD | I    | <b>Power Good (Power-on Reset).</b> The Power Good signal is used to indicate that stable power is available for the 82540EP. When the signal is low, the 82540EP holds itself in reset state and floats all PCI signals.                                                               |
| PME#         | OD   | <b>Power Management Event.</b> The 82540EP device drives this signal low when it receives a wake-up event and either the PME Enable bit in the Power Management Control/Status Register or the Advanced Power Management Enable (APME) bit of the Wake-up Control Register (WUC) is 1b. |
| AUX_PWR      | I    | <b>Auxiliary Power.</b> If the Auxiliary Power signal is high, then auxiliary power is available and the 82540EP device should support the D3cold power state.                                                                                                                          |

### 3.2.7 Impedance Compensation Signals

| Symbol  | Type | Name and Function                                                                                                                                                                                                                                                                      |
|---------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ZN_COMP | I/O  | <b>N Device Impedance Compensation.</b> This signal should be connected to an external precision resistor (to VDD) that is indicative of the PCI trace load. This cell is used to dynamically determine the drive strength required on the N-channel transistors in the PCI I/O cells. |
| ZP_COMP | I/O  | <b>P Device Impedance Compensation.</b> This signal should be connected to an external precision resistor (to VSS) that is indicative of the PCI trace load. This cell is used to dynamically determine the drive strength required on the P-channel transistors in the PCI I/O cells. |

### 3.2.8 SMB Signals

| Symbol     | Type | Name and Function                                                                        |
|------------|------|------------------------------------------------------------------------------------------|
| SMBCLK     | I/O  | <b>SMB Clock.</b> The SMB Clock signal is an open drain signal for serial SMB interface. |
| SMBDATA    | I/O  | <b>SMB Data.</b> The SMB Data signal is an open drain signal for serial SMB interface.   |
| SMB_ALERT# | O    | <b>SMB Alert.</b> The SMB Alert signal is open drain for serial SMB interface.           |

## 3.3 EEPROM and Serial FLASH Interface Signals

| Symbol | Type | Name and Function                                                                                                                                |
|--------|------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| EEDI   | O    | <b>EEPROM Data Input.</b> The EEPROM Data Input pin is used for output to the memory device.                                                     |
| EEDO   | I    | <b>EEPROM Data Output.</b> The EEPROM Data Output pin is used for input from the memory device. The EE_DO includes an internal pull-up resistor. |
| EECS   | O    | <b>EEPROM Chip Select.</b> The EEPROM Chip Select signal is used to enable the device.                                                           |
| EESK   | O    | <b>EEPROM Serial Clock.</b> The EEPROM Shift Clock provides the clock rate for the EEPROM interface, which is approximately 1 MHz.               |



| Symbol  | Type | Name and Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|---------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| FL_CE#  | O    | <b>FLASH Chip Enable Output.</b> Used to enable FLASH device.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| FL_SCK  | O    | <b>FLASH Serial Clock Output.</b> The clock rate of the serial FLASH interface is approximately 1 MHz.                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| FL_SI   | O    | <b>FLASH Serial Data Input.</b> This pin is an output to the memory device.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| FLSH_SO | I    | <b>FLASH Serial Data Output.</b> This pin is an input from the FLASH memory.<br><b>Note:</b> The 82540EP LAN-disable mechanism is implemented using this pin. It is generally used when no Flash device is present (Flash disabled). If this pin is 1b (Vcc) then the 82540EP is enabled. If the pin is 0b (Vss) then the 82540EP is disabled. This signal should be sampled within 1µs of the rising edge of LAN_PWR_GOOD and PCI_RST_N. Note that this pin also has an internal pull-up that is sufficient enough to enable the 82540EP if no Flash device is present. |

*Note:* If the LAN-disable feature is used when a Flash device is present, then care must be taken by system designers not to drive the FLSH\_SO pin while the Flash device is driving it.

### 3.4 Miscellaneous Signals

#### 3.4.1 LED Signals

| Symbol    | Type | Name and Function                                                                                                |
|-----------|------|------------------------------------------------------------------------------------------------------------------|
| LINK_UP#  | O    | <b>LED0 / LINK Up.</b> Programmable LED indication. Defaults to indicate link connectivity.                      |
| ACTIVITY# | O    | <b>LED1 / Activity.</b> Programmable LED indication. Defaults to flash to indicate transmit or receive activity. |
| LINK100#  | O    | <b>LED2 / LINK 100.</b> Programmable LED indication. Defaults to indicate link at 100 Mbps.                      |
| LINK1000# | O    | <b>LED3 / LINK 1000.</b> Programmable LED indication. Defaults to indicate link at 1000 Mbps.                    |

#### 3.4.2 Other Signals

| Symbol               | Type | Name and Function                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SDP[7:6]<br>SDP[1:0] | TS   | <b>Software Defined Pins.</b> The Software Defined Pins are reserved and programmable with respect to input and output capability. These default to input signals upon power-up but may be configured differently by the EEPROM. The upper four bits may be mapped to the General Purpose Interrupt bits if they are configured as input signals.<br><b>Note:</b> SDP5 is not included in the group of Software Defined Pins. |

## 3.5 PHY Signals

### 3.5.1 Crystal Signals

| Symbol | Type | Name and Function                                                                                                                                                                                      |
|--------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| XTAL1  | I    | <b>Crystal One.</b> The Crystal One pin is a 25 MHz +/- 30 ppm input signal. It can be connected to either an oscillator or crystal. If a crystal is used, Crystal Two (XTAL2) must also be connected. |
| XTAL2  | O    | <b>Crystal Two.</b> Crystal Two is the output of an internal oscillator circuit used to drive a crystal into oscillation. If an external oscillator is used in the design, XTAL2 must be disconnected. |

### 3.5.2 Analog Signals

| Symbol    | Type | Name and Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REF       | P    | <b>Reference.</b> This Reference signal should be connected to VSS through an external 2.49 K $\Omega$ resistor.                                                                                                                                                                                                                                                                                                                                                                                   |
| MDI[0]+/- | A    | <b>Media Dependent Interface [0].</b><br><b>100BASE-T:</b> In MDI configuration, MDI[0]+/- corresponds to BI_DA+/-, and in MDI-X configuration, MDI[0]+/- corresponds to BI_DB+/-.<br><b>100BASE-TX:</b> In MDI configuration, MDI[0]+/- is used for the transmit pair, and in MDI-X configuration, MDI[0]+/- is used for the receive pair.<br><b>10BASE-T:</b> In MDI configuration, MDI[0]+/- is used for the transmit pair, and in MDI-X configuration, MDI[0]+/- is used for the receive pair. |
| MDI[1]+/- | A    | <b>Media Dependent Interface [1].</b><br><b>100BASE-T:</b> In MDI configuration, MDI[1]+/- corresponds to BI_DB+/-, and in MDI-X configuration, MDI[1]+/- corresponds to BI_DA+/-.<br><b>100BASE-TX:</b> In MDI configuration, MDI[1]+/- is used for the receive pair, and in MDI-X configuration, MDI[1]+/- is used for the transmit pair.<br><b>10BASE-T:</b> In MDI configuration, MDI[1]+/- is used for the receive pair, and in MDI-X configuration, MDI[1]+/- is used for the transmit pair. |
| MDI[2]+/- | A    | <b>Media Dependent Interface [2].</b><br><b>100BASE-T:</b> In MDI configuration, MDI[2]+/- corresponds to BI_DC+/-, and in MDI-X configuration, MDI[2]+/- corresponds to BI_DD+/-.<br><b>100BASE-TX:</b> Unused.<br><b>10BASE-T:</b> Unused.                                                                                                                                                                                                                                                       |
| MDI[3]+/- | A    | <b>Media Dependent Interface [3].</b><br><b>100BASE-T:</b> In MDI configuration, MDI[3]+/- corresponds to BI_DD+/-, and in MDI-X configuration, MDI[3]+/- corresponds to BI_DC+/-.<br><b>100BASE-TX:</b> Unused.<br><b>10BASE-T:</b> Unused.                                                                                                                                                                                                                                                       |

## 3.6 Test Interface Signals

| Symbol     | Type | Name and Function                                                                                                                                                       |
|------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| JTAG_TCK   | I    | <b>JTAG Clock.</b>                                                                                                                                                      |
| JTAG_TDI   | I    | <b>JTAG TDI.</b>                                                                                                                                                        |
| JTAG_TDO   | O    | <b>JTAG TDO.</b>                                                                                                                                                        |
| JTAG_TMS   | I    | <b>JTAG TMS.</b>                                                                                                                                                        |
| JTAG_TRST# | I    | <b>JTAG Reset.</b> This is an active low reset signal for JTAG. This signal should be terminated using a pull-down resistor to ground. It must not be left unconnected. |
| TEST       | I    | <b>Factory Test Pin.</b>                                                                                                                                                |
| CLK_VIEW   | O    | <b>Clock View.</b> Output for GTX_CLK and RX_CLK during IEEE PHY conformance testing. The clock is selected by register programming.                                    |
| ALTCLK_125 | I    | <b>Alternate CLK125 Input.</b> Factory use only.<br>For normal component operation, connect to VSS.                                                                     |
| CLK_BYP#   | I    | <b>Clock Bypass Enable.</b> Factory use only.<br>For normal component operation, no connect.                                                                            |
| HSDACP     | I    | <b>PHY High Speed Test Interface.</b> Factory use only.<br>For normal component operation, no connect.                                                                  |
| HSDACN     | I    | <b>PHY High Speed Test Interface.</b> Factory use only.<br>For normal component operation, no connect.                                                                  |
| PHY_TSTPT  | I    | <b>PHY Test Point.</b> Factory use only.<br>For normal component operation, no connect.                                                                                 |

## 3.7 Power Supply Connections

### 3.7.1 Digital Supplies

| Symbol | Type | Name and Function                       |
|--------|------|-----------------------------------------|
| VDDO   | P    | <b>3.3 V I/O Power Supply.</b>          |
| DVDD   | P    | <b>1.5 V Digital Core Power Supply.</b> |

### 3.7.2 Analog Supplies

| Symbol | Type | Name and Function                 |
|--------|------|-----------------------------------|
| AVDDH  | P    | <b>3.3 V Analog Power Supply.</b> |
| AVDDL  | P    | <b>2.5 V Analog Power Supply.</b> |

### 3.7.3 Ground and No Connects

| Symbol | Type | Name and Function                                                                                                                    |
|--------|------|--------------------------------------------------------------------------------------------------------------------------------------|
| GND    | P    | <b>Ground.</b>                                                                                                                       |
| NC     | P    | <b>No Connect.</b> Do not connect any circuitry to these pins. Pull-up or pull-down resistors should not be connected to these pins. |

### 3.7.4 Control Signals

| Symbol | Type | Name and Function                                                                                                                                                                                                                                                                                            |
|--------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CTRL15 | A    | <b>1.5V Control.</b> LDO voltage regulator output to drive external pass transistor. If 1.5 V is already present in the system, leave output unconnected. To achieve optimal D <sub>3</sub> power consumption (<50 mw), leave the output unconnected and use a high-efficiency external switching regulator. |
| CTRL25 | A    | <b>2.5V Control.</b> LDO voltage regulator output to drive external pass transistor. If 2.5 V is already present in the system, leave output unconnected. To achieve optimal D <sub>3</sub> power consumption (<50 mw), leave the output unconnected and use a high-efficiency external switching regulator. |

## 4.0 Voltage, Temperature, and Timing Specifications

**Note:** The specification values listed in this section are subject to change without notice. Verify with your local Intel sales office that you have the latest information before finalizing a design.

### 4.1 Absolute Maximum Ratings

**Table 1. Absolute Maximum Ratings<sup>a</sup>**

| Symbol    | Parameter            | Min  | Max            | Unit |
|-----------|----------------------|------|----------------|------|
| $V_{DD}$  | DC supply voltage    | -0.3 | 7              | V    |
| $V_{IN}$  | Input voltage        | -1   | $V_{DD} + 0.3$ | V    |
| $I_{IN}$  | DC input pin current | -10  | 10             | mA   |
| $T_{STG}$ | Storage temperature  | -40  | 125            | °C   |

a. Maximum ratings are referenced to ground (VSS). Permanent device damage is likely to occur if the ratings in this table are exceeded. These values should not be used as the limits for normal device operations.

### 4.2 Recommended Operating Conditions

**Table 2. Recommended Operating Conditions<sup>a</sup> (Sheet 1 of 2)**

| Symbol   | Parameter               | Condition               | Min | Typ | Max  | Unit |
|----------|-------------------------|-------------------------|-----|-----|------|------|
| $T_{OP}$ | Operating Temperature   |                         | -40 |     | 85   | °C   |
| $V_{IO}$ | VIO Voltage Range       |                         | 3   |     | 5.25 | V    |
| $V_{DD}$ | Periphery Voltage Range | $3.3\text{ V} \pm 10\%$ | 3   | 3.3 | 3.6  | V    |

Table 2. Recommended Operating Conditions<sup>a</sup> (Sheet 2 of 2)

| Symbol          | Parameter                  | Condition   | Min   | Typ | Max   | Unit |
|-----------------|----------------------------|-------------|-------|-----|-------|------|
| V <sub>AH</sub> | Analog High VDD Range      | 3.3 V ± 10% | 3     | 3.3 | 3.6   | V    |
| V <sub>D</sub>  | Core Digital Voltage Range | 1.5 V ± 5%  | 1.425 | 1.5 | 1.575 | V    |
| V <sub>AL</sub> | Analog Low VDD Range       | 2.5 V ± 5%  | 2.375 | 2.5 | 2.625 | V    |

a. Sustained operation of the device at conditions exceeding these values, even if they are within the absolute maximum rating limits, might result in permanent damage.

## 4.3 DC Specifications

Table 3. DC Characteristics

| Symbol                | Parameter                          | Min  | Typ | Max  | Units |
|-----------------------|------------------------------------|------|-----|------|-------|
| V <sub>DD</sub> (3.3) | DC supply voltage on VD00 or AVDDH | 3.00 | 3.3 | 3.60 | V     |
| V <sub>DD</sub> (2.5) | DC supply voltage on AVDDL         | 2.38 | 2.5 | 2.62 | V     |
| V <sub>DD</sub> (1.5) | DC supply voltage on DVDD          | 1.43 | 1.5 | 1.57 | V     |

Table 4. Power Specifications - D0a

|                    | D0a                      |                          |                          |                          |                          |                          |                          |                          |
|--------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
|                    | unplugged/no link        |                          | @10 Mbps                 |                          | @100Mbps                 |                          | @1000Mbps                |                          |
|                    | Typ I <sub>cc</sub> (mA) | Max I <sub>cc</sub> (mA) | Typ I <sub>cc</sub> (mA) | Max I <sub>cc</sub> (mA) | Typ I <sub>cc</sub> (mA) | Max I <sub>cc</sub> (mA) | Typ I <sub>cc</sub> (mA) | Max I <sub>cc</sub> (mA) |
| 3.3 V              | 40                       | 40                       | 55                       | 65                       | 65                       | 80                       | 125                      | 125                      |
| 2.5 V              | 20                       | 20                       | 30                       | 35                       | 55                       | 60                       | 145                      | 150                      |
| 1.5 V              | 100                      | 120                      | 95                       | 100                      | 115                      | 125                      | 400                      | 425                      |
| Total Device Power | 325 mW                   |                          | 400 mW                   |                          | 525 mW                   |                          | 1.38 W                   | 1.5 W                    |

**Table 5. Power Specifications - D3cold**

|                           | D3cold - wake-up enabled |              |              |              |              |              | D3cold - wake disabled - max power savings mode disabled |              | D3cold - wake disabled - max power savings mode enabled <sup>a</sup> |              |
|---------------------------|--------------------------|--------------|--------------|--------------|--------------|--------------|----------------------------------------------------------|--------------|----------------------------------------------------------------------|--------------|
|                           | unplugged/no link        |              | @10 Mbps     |              | @100Mbps     |              |                                                          |              |                                                                      |              |
|                           | Typ lcc (mA)             | Max lcc (mA) | Typ lcc (mA) | Max lcc (mA) | Typ lcc (mA) | Max lcc (mA) | Typ lcc (mA)                                             | Max lcc (mA) | Typ lcc (mA)                                                         | Max lcc (mA) |
| 3.3 V                     | 40                       | 40           | 55           | 55           | 50           | 50           | 40                                                       | 40           | 6                                                                    | 8            |
| 2.5 V                     | 20                       | 20           | 30           | 30           | 55           | 55           | 20                                                       | 20           | 0.1                                                                  | 0.1          |
| 1.5 V                     | 40                       | 40           | 30           | 35           | 55           | 60           | 10                                                       | 10           | 1                                                                    | 1            |
| <b>Total Device Power</b> | 240 mW                   |              | 300 mW       |              | 385 mW       |              | 195 mW                                                   |              | 20 mW                                                                |              |

a. Special Note: To obtain the benefit of max power savings mode, do not use the internal voltage regulator control circuit and external pass transistors. Use external switching regulators for highest efficiency.

**Table 6. Power Specifications D(r) Uninitialized**

|                           | D(r) Uninitialized<br>(LAN_PWR_GOOD=0) |              |
|---------------------------|----------------------------------------|--------------|
|                           | Typ lcc (mA)                           | Max lcc (mA) |
| 3.3 V                     | 40                                     | 45           |
| 2.5 V                     | 40                                     | 45           |
| 1.5 V                     | 190                                    | 200          |
| <b>Total Device Power</b> | 520 mW                                 |              |

**Table 7. Power Specifications - Complete Subsystem**

|       | Complete Subsystem (Reference Design)<br>Including Magnetics, LED, Regulator Circuits |              |                             |              |                              |              |                     |              |                                                         |              |
|-------|---------------------------------------------------------------------------------------|--------------|-----------------------------|--------------|------------------------------|--------------|---------------------|--------------|---------------------------------------------------------|--------------|
|       | D3cold - wake disabled - max power savings mode disabled                              |              | D3cold wake-enabled @10Mbps |              | D3cold wake-enabled @100Mbps |              | D0 @1000Mbps active |              | D3cold - wake disabled - max power savings mode enabled |              |
|       | Typ lcc (mA)                                                                          | Max lcc (mA) | Typ lcc (mA)                | Max lcc (mA) | Typ lcc (mA)                 | Max lcc (mA) | Typ lcc (mA)        | Max lcc (mA) | Typ lcc (mA)                                            | Max lcc (mA) |
| 3.3 V | 40                                                                                    | 40           | 60                          | 60           | 60                           | 60           | 130                 | 130          | 6                                                       | 8            |

Table 7. Power Specifications - Complete Subsystem

|                            |    |       |    |        |    |        |     |        |     |       |
|----------------------------|----|-------|----|--------|----|--------|-----|--------|-----|-------|
| 2.5 V                      | 20 | 20    | 40 | 40     | 80 | 80     | 240 | 245    | 0.1 | 0.1   |
| 1.5 V                      | 10 | 10    | 30 | 35     | 55 | 60     | 400 | 425    | 1   | 1     |
| Subsystem<br>3.3 V current |    | 70 mA |    | 135 mA |    | 200 mA |     | 800 mA |     | 10 mA |

Table 8. I/O Characteristics

| Symbol     | Parameter                         | Condition                           | Min  | Typ     | Max            | Unit       |
|------------|-----------------------------------|-------------------------------------|------|---------|----------------|------------|
| $V_{IL}$   | Voltage input LOW                 |                                     | -0.5 |         | 0.8            | V          |
| $V_{IH}$   | Voltage input HIGH                |                                     | 2    |         | $V_{DD} + 0.3$ | V          |
| $V_{OL}$   | Voltage output LOW                |                                     |      |         | 0.4            | V          |
| $V_{OH}$   | Voltage output HIGH               |                                     | 2.4  |         |                | V          |
| $V_{SH}$   | Schmitt Trigger Hysteresis        |                                     | 0.1  |         |                | V          |
| $I_{OL}^a$ | Output current LOW                |                                     |      |         |                |            |
|            | 3mA drivers (TTL3)                | $V_{OL}$                            | 3    |         |                | mA         |
|            | 6mA drivers (TTL6)                | $V_{OL}$                            | 6    |         |                | mA         |
|            | 12mA drivers (TTL12)              | $V_{OL}$                            | 12   |         |                | mA         |
| $I_{OH}^a$ | Output current HIGH               |                                     |      |         |                |            |
|            | 3mA drivers (TTL3)                | $V_{OH}$                            | -3   |         |                | mA         |
|            | 6mA drivers (TTL6)                | $V_{OH}$                            | -6   |         |                | mA         |
|            | 12mA drivers (TTL12)              | $V_{OH}$                            | -12  |         |                | mA         |
| $I_{IN}$   | Input Current                     | $V_{IN} = V_{DD}$ or $V_{SS}$       | -10  | $\pm 1$ | 10             | $\mu A$    |
|            | TTL inputs                        | $V_{IN} = V_{DD}$                   | 150  |         | 480            | $\mu A$    |
|            | Inputs with pull-down resistors   | $V_{IN} = V_{SS}$                   | -150 |         | -480           | $\mu A$    |
|            | TTL inputs with pull-up resistors |                                     |      |         |                |            |
| $I_{OZ}$   | 3-state output leakage current    | $V_{OH} = V_{DD}$ or $V_{SS}$       | -10  | $\pm 1$ | 10             | $\mu A$    |
| $C_{IN}$   | Input capacitance                 | Any input and bi-directional buffer |      | 2.5     |                | pF         |
| $C_{OUT}$  | Output capacitance                | Any output buffer                   |      | 2       |                | pF         |
| $C_{PUD}$  | Pull-up/down Resistor value       |                                     | 15   | 20      | 30             | k $\Omega$ |

a. TTL3 signals include: EE\_DI, EE\_SK, EE\_CS, and JTAG\_TDO.

TTL6 signals include: CLKRUN#, FL\_CE#, FL\_SCK, FL\_SI, and CLK\_VIEW.

TTL12 signals include: LED0 / LINK #, LED1 / ACT #, LED2 / LINK100 #, LED3 / LINK1000 #, SDP0, SDP1, SDP6, and SDP7.



## 4.4 AC Characteristics

**Table 9. AC Characteristics: 3.3 V Interfacing**

| Symbol | Parameter                   | Min | Typ | Max | Unit |
|--------|-----------------------------|-----|-----|-----|------|
| CLK    | Clock frequency in PCI mode |     |     | 66  | MHz  |

**Table 10. 25 MHz Clock Input Requirements**

| Symbol    | Parameter <sup>a</sup> | Min         | Typ | Max         | Unit |
|-----------|------------------------|-------------|-----|-------------|------|
| fi_TX_CLK | TX_CLK_IN frequency    | 25 - 50 ppm | 25  | 25 + 50 ppm | MHz  |

a. This parameter applies to an oscillator connected to the Crystal One (XTAL1) input. Alternatively, a crystal may be connected to XTAL1 and XTAL2 as the frequency source for the internal oscillator.

**Table 11. Link Interface Clock Requirements**

| Symbol            | Parameter         | Min | Typ | Max | Unit |
|-------------------|-------------------|-----|-----|-----|------|
| fGTX <sup>a</sup> | GTX_CLK frequency |     | 125 |     | MHz  |

a. GTX\_CLK is used externally for test purposes only.

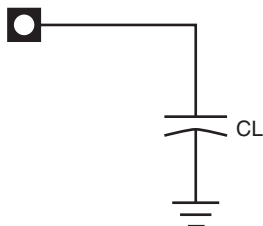
**Table 12. EEPROM Interface Clock Requirements**

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|-----------|-----|-----|-----|------|
| fSK    |           |     |     | 1   | MHz  |

**Table 13. AC Test Loads for General Output Pins**

| Symbol | Signal Name                       | Value | Units |
|--------|-----------------------------------|-------|-------|
| CL     | TDO                               | 10    | pF    |
| CL     | PME#, SDP[7:0]                    | 16    | pF    |
| CL     | EEDI, EESK                        | 18    | pF    |
| CL     | RX_ACTIVITY, TX_ACTIVITY, LINK_UP | 20    | pF    |

Figure 1. AC Test Loads for General Output Pins



## 4.5 Timing Specifications

**Note:** Timing specifications are subject to change. Verify with your local Intel sales office that you have the latest information before finalizing a design.

### 4.5.1 PCI Bus Interface

#### 4.5.1.1 PCI Bus Interface Clock

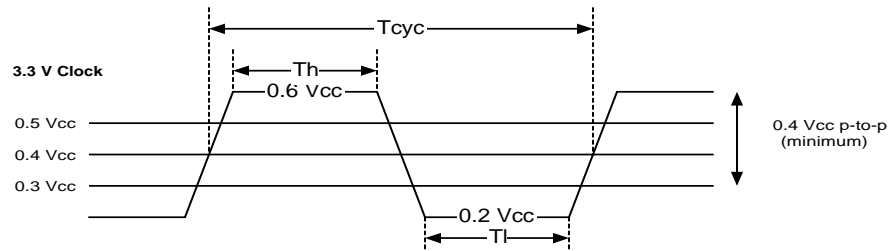
Table 14. PCI Bus Interface Clock Parameters

| Symbol | Parameter <sup>a</sup>      | PCI 66 MHz |     | PCI 33 MHz |     | Units |
|--------|-----------------------------|------------|-----|------------|-----|-------|
|        |                             | Min        | Max | Min        | Max |       |
| TCYC   | CLK cycle time              | 15         | 30  | 30         |     | ns    |
| TH     | CLK high time               | 6          |     | 11         |     | ns    |
| TL     | CLK low time                | 6          |     | 11         |     | ns    |
|        | CLK slew rate               | 1.5        | 4   | 1          | 4   | V/ns  |
|        | RST# slew rate <sup>b</sup> | 50         |     | 50         |     | mV/ns |

a. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown.

b. The minimum RST# slew rate applies only to the rising (de-assertion) edge of the reset signal and ensures that system noise cannot render a monotonic signal to appear bouncing in the switching range.

Figure 2. PCI Clock Timing



#### 4.5.1.2 PCI Bus Interface Timing

Table 15. PCI Bus Interface Timing Parameters

| Symbol    | Parameter                                         | PCI 66MHz          |     | PCI 33 MHz         |     | Units |
|-----------|---------------------------------------------------|--------------------|-----|--------------------|-----|-------|
|           |                                                   | Min                | Max | Min                | Max |       |
| TVAL      | CLK to signal valid delay: bussed signals         | 2                  | 6   | 2                  | 11  | ns    |
| TVAL(ptp) | CLK to signal valid delay: point-to-point signals | 2                  | 6   | 2                  | 12  | ns    |
| TON       | Float to active delay                             | 2                  |     | 2                  |     | ns    |
| TOFF      | Active to float delay                             |                    | 14  |                    | 28  | ns    |
| TSU       | Input setup time to CLK: bussed signals           | 3                  |     | 7                  |     | ns    |
| TSU(ptp)  | Input setup time to CLK: point-to-point signals   | 5                  |     | 10, 12             |     | ns    |
| TH        | Input hold time from CLK                          | 0                  |     | 0                  |     | ns    |
| TRRSU     | REQ64# to RST# setup time                         | $10 \cdot T_{CYC}$ |     | $10 \cdot T_{CYC}$ |     | ns    |
| TRRH      | RST# to REQ64# hold time                          | 0                  |     | 0                  |     | ns    |

**NOTES:**

1. Output timing measurements are as shown.
2. REQ# and GNT# signals are point-to-point and have different output valid delay and input setup times than bussed signals. GNT# has a setup of 10 ns; REQ# has a setup of 12 ns. All other signals are bussed.
3. Input timing measurements are as shown.

Figure 3. PCI Bus Interface Output Timing Measurement

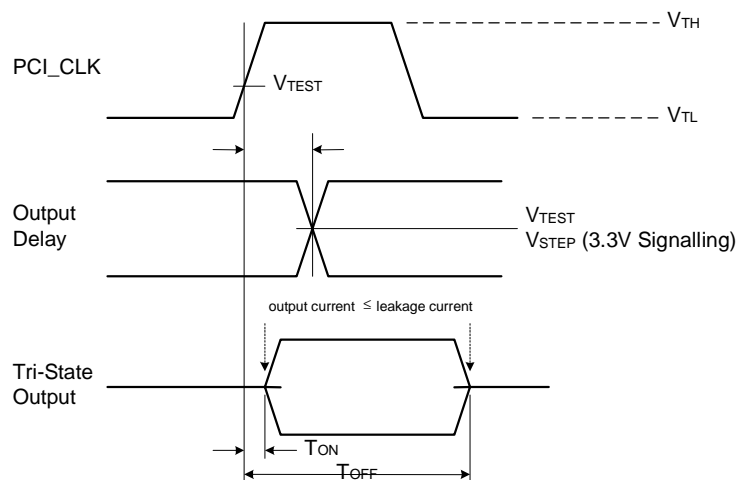


Figure 4. PCI Bus Interface Input Timing Measurement Conditions

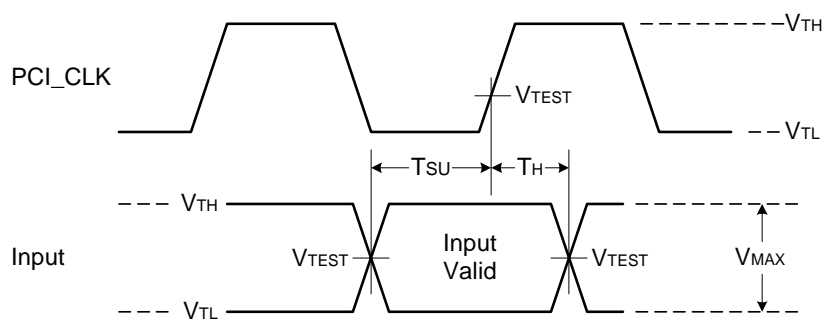


Table 16. PCI Bus Interface Timing Measurement Conditions

| Symbol     | Parameter                             | PCI 66 MHz<br>3.3 v | Unit |
|------------|---------------------------------------|---------------------|------|
| $V_{TH}$   | Input measurement test voltage (high) | $0.6 \cdot V_{CC}$  | V    |
| $V_{TL}$   | Input measurement test voltage (low)  | $0.2 \cdot V_{CC}$  | V    |
| $V_{TEST}$ | Output measurement test voltage       | $0.4 \cdot V_{CC}$  | V    |
|            | Input signal slew rate                | 1.5                 | V/ns |

Figure 5. TVAL (max) Rising Edge Test Load

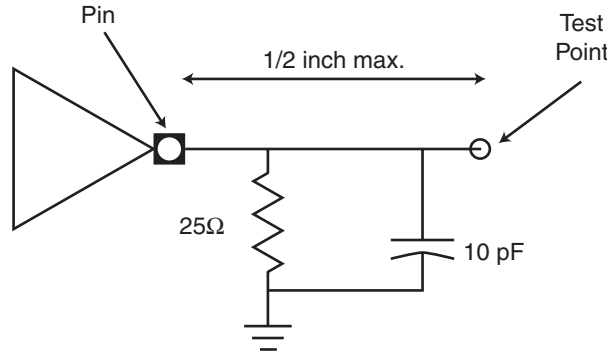


Figure 6. TVAL (max) Falling Edge Test Load

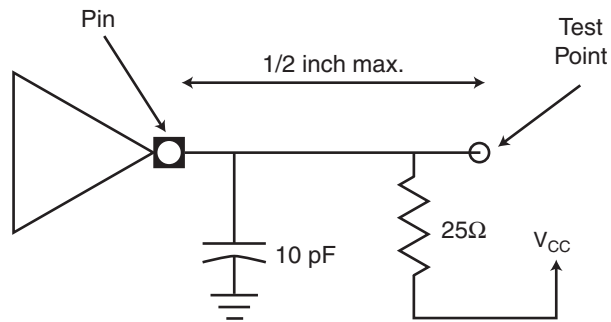


Figure 7. TVAL (min) Test Load

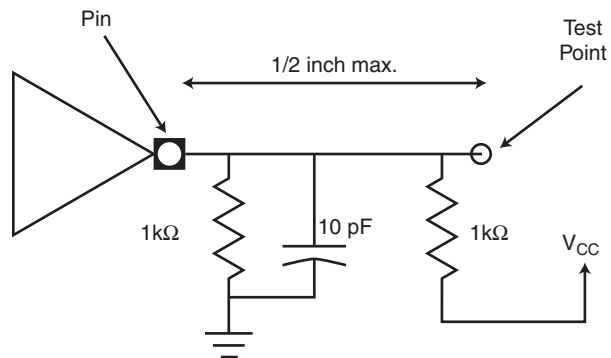
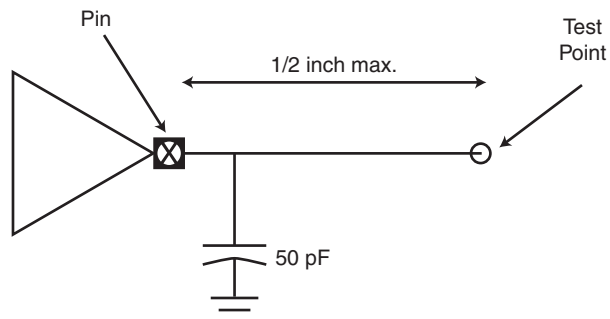


Figure 8. TVAL Test Load (PCI 5 V Signaling Environment)



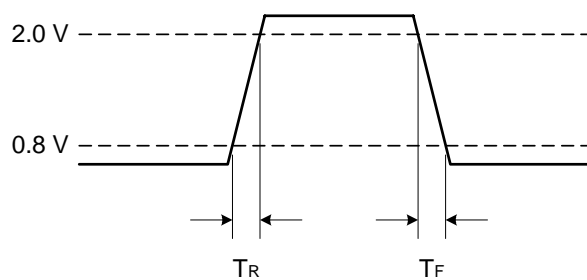
NOTE: Note: 50 pF load used for maximum times. Minimum times are specified with 0 pF load.

### 4.5.2 Link Interface Timing

Table 17. Rise and Fall Times

| Symbol | Parameter       | Condition      | Min | Max | Unit |
|--------|-----------------|----------------|-----|-----|------|
| TR     | Clock rise time | 0.8 V to 2.0 V | 0.7 |     | ns   |
| TF     | Clock fall time | 2.0 V to 0.8 V | 0.7 |     | ns   |
| TR     | Data rise time  | 0.8 to 2.0 V   | 0.7 |     | ns   |
| TF     | Data fall time  | 2.0 V to 0.8 V | 0.7 |     | ns   |

Figure 9. Link Interface Rise/Fall Timing



### 4.5.3 EEPROM Interface

**Table 18. Link Interface Clock Requirements**

| Symbol | Parameter        | Min | Typ         | Max | Unit |
|--------|------------------|-----|-------------|-----|------|
| TPW    | EESK pulse width |     | TPERIOD*128 |     | ns   |

a. The EEPROM clock is derived from a 125 MHz internal clock.

**Table 19. Link Interface Clock Requirements**

| Symbol | Parameter <sup>a</sup> | Min    | Typ | Max | Unit |
|--------|------------------------|--------|-----|-----|------|
| TDOS   | EEDO setup time        | TCYC*2 |     |     | ns   |
| TDOH   | EEDO hold time         | 0      |     |     | ns   |

a. The EEDO setup and hold time is a function of the PCI bus CLK cycle time but is referenced to EESK.



*Note:* This page intentionally left blank.



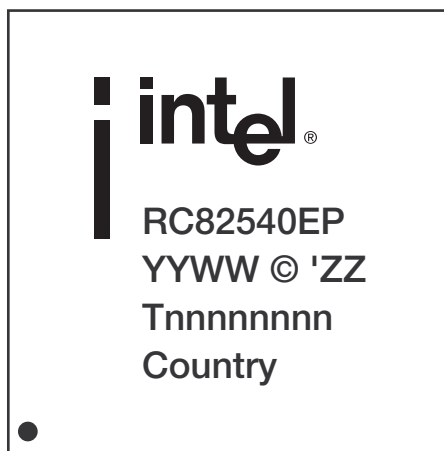
## 5.0 Package and Pinout Information

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This section describes the 82540EP device, manufactured in a 196-lead ball grid array measuring 15mm X 15mm. External product identification is shown in Figure 10. The nominal ball pitch is 1mm. The pin number-to-signal mapping is indicated beginning with Table 19.

### 5.1 Device Identification

Figure 10. 82540EP Device Identification Markings



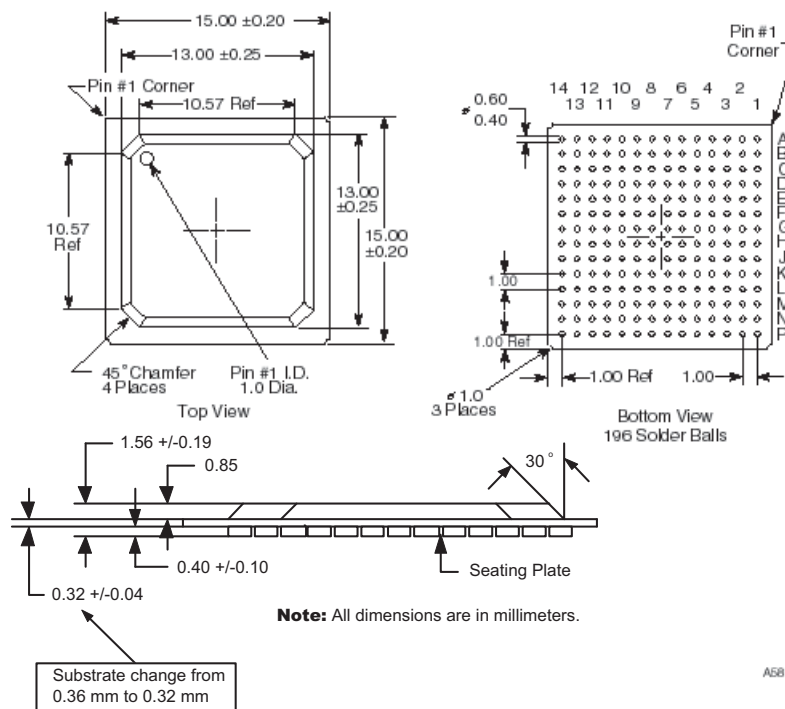
|           |                            |
|-----------|----------------------------|
| 82540EP   | Product Name               |
| YYWW      | Date Code                  |
| Tnnnnnnnn | Lot Trace Code             |
| (c)'ZZ    | Copyright Information      |
| Country   | Country of Origin Assembly |

**NOTE:** “●” indicates the location of pin 1. It is not an actual mark on the device

## 5.2 Package Information

The 82540EP device is a 196-lead ball grid array (TFBGA) measuring 15 mm<sup>2</sup>. The package dimensions are detailed in Figure 11. The nominal ball pitch is 1 mm. .

**Figure 11. Dimension Diagram for the 196-pin BGA**



**Note:** No changes to existing soldering processes are needed for the 0.32 mm substrate change.

### 5.3 Thermal Specifications

The 82540EP device is specified for operation when the ambient temperature (TA) is within the range of 0° C to 70° C.

TC (case temperature) is calculated using the equation:

$$TC = TA + P (\theta JA - q JC)$$

TJ (junction temperature) is calculated using the equation:

$$TJ = TA + P \theta JA$$

P (power consumption) is calculated by using the typical ICC, as indicated in Table 4 of Section 4.0, and nominal VCC. The thermal resistances are shown in Table 18.

**Table 18. Thermal Characteristics**

| Symbol      | Parameter                               | Value at specified airflow (m/s) |      |      |      | Units       |
|-------------|-----------------------------------------|----------------------------------|------|------|------|-------------|
|             |                                         | 0                                | 1    | 2    | 3    |             |
| $\theta JA$ | Thermal resistance, junction-to-ambient | 28.1                             | 25.0 | 23.7 | 22.8 | °C/<br>Watt |
| $\theta JC$ | Thermal resistance, junction-to-case    | 6.1                              | 6.1  | 6.1  | 6.1  | °C/<br>Watt |

Thermal resistances are determined empirically with test devices mounted on standard thermal test boards. Real system designs may have different characteristics due to board thickness, arrangement of ground planes, and proximity of other components. The case temperature measurements should be used to assure that the 82540EP device is operating under recommended conditions.

## 5.4 Pinout Information

**Table 19. PCI Address, Data, and Control Signals**

| Signal | Pin | Signal | Pin | Signal   | Pin |
|--------|-----|--------|-----|----------|-----|
| AD[0]  | N7  | AD[16] | K1  | C/BE#[0] | M4  |
| AD[1]  | M7  | AD[17] | E3  | C/BE#[1] | L3  |
| AD[2]  | P6  | AD[18] | D1  | C/BE#[2] | F3  |
| AD[3]  | P5  | AD[19] | D2  | C/BE#[3] | C4  |
| AD[4]  | N5  | AD[20] | D3  | PAR      | J1  |
| AD[5]  | M5  | AD[21] | C1  | FRAME#   | F2  |
| AD[6]  | P4  | AD[22] | B1  | IRDY#    | F1  |
| AD[7]  | N4  | AD[23] | B2  | TRDY#    | G3  |
| AD[8]  | P3  | AD[24] | B4  | STOP#    | H1  |
| AD[9]  | N3  | AD[25] | A5  | DEVSEL#  | H3  |
| AD[10] | N2  | AD[26] | B5  | VIO      | G2  |
| AD[11] | M1  | AD[27] | B6  | IDSEL    | A4  |
| AD[12] | M2  | AD[28] | C6  |          |     |
| AD[13] | M3  | AD[29] | C7  |          |     |
| AD[14] | L1  | AD[30] | A8  |          |     |
| AD[15] | L2  | AD[31] | B8  |          |     |

**Table 20. PCI Arbitration Signals**

| Signal | Pin |
|--------|-----|
| REQ#   | C3  |
| GNT#   | J3  |

**Table 21. Interrupt Signals**

| Signal | Pin |
|--------|-----|
| INTA#  | H2  |

**Table 22. System Signals**

| Signal | Pin | Signal | Pin | Signal | Pin |
|--------|-----|--------|-----|--------|-----|
| CLK    | G1  | M66EN  | C2  | RST#   | B9  |

**Table 23. Error Reporting Signals**

| Signal | Pin | Signal | Pin |
|--------|-----|--------|-----|
| SERR#  | A2  | PERR#  | J2  |

**Table 24. Power Management Signals**

| Signal       | Pin | Signal   | Pin |
|--------------|-----|----------|-----|
| LAN_PWR_GOOD | A9  | AUX_PWR  | J12 |
| PME#         | A6  | CLK_RUN# | C8  |

**Table 25. Impedance Compensation Signals**

| Signal  | Pin | Signal  | Pin |
|---------|-----|---------|-----|
| ZN_COMP | H4  | ZP_COMP | G4  |

**Table 26. SMB Signals**

| Signal | Pin | Signal  | Pin | Signal     | Pin |
|--------|-----|---------|-----|------------|-----|
| SMBCLK | A10 | SMBDATA | C9  | SMB_ALERT# | B10 |

**Table 27. EEPROM and Serial FLASH Interface Signals**

| Signal | Pin | Signal | Pin | Signal  | Pin |
|--------|-----|--------|-----|---------|-----|
| EESK   | M10 | EEDI   | P10 | FL_SCK  | N9  |
| EEDO   | N10 | FL_CE# | M9  | FLSH_SO | P9  |
| EECS   | P7  | FL_SI  | M11 |         |     |

**Table 28. LED Signals**

| Signal    | Pin | Signal    | Pin |
|-----------|-----|-----------|-----|
| LINK_UP#  | A12 | LINK100#  | B11 |
| ACTIVITY# | C11 | LINK1000# | B12 |

**Table 29. Other Signals**

| Signal | Pin | Signal | Pin | Signal | Pin |
|--------|-----|--------|-----|--------|-----|
| SDP[0] | N14 | SDP[6] | N13 | CTRL15 | P11 |
| SDP[1] | P13 | SDP[7] | M12 | CTRL25 | B13 |

**Table 30. IEEE Test Signals**

| Signal   | Pin |
|----------|-----|
| CLK_VIEW | M8  |

Table 31. PHY Signals

| Signal  | Pin | Signal  | Pin | Signal  | Pin |
|---------|-----|---------|-----|---------|-----|
| XTAL1   | K14 | MDI[0]+ | C13 | MDI[2]+ | F13 |
| XTAL2   | J14 | MDI[1]- | E14 | MDI[3]- | H14 |
| REF     | B14 | MDI[1]+ | E13 | MDI[3]+ | H13 |
| MDI[0]- | C14 | MDI[2]- | F14 |         |     |

Table 32. Test Interface Signals

| Signal   | Pin | Signal   | Pin | Signal    | Pin |
|----------|-----|----------|-----|-----------|-----|
| JTAG_TCK | L14 | JTAG_TDO | M14 | JTAG_RST# | L13 |
| JTAG_TDI | M13 | JTAG_TMS | L12 | TEST      | A13 |

Table 33. Digital Power Signals

| Signal      | Pin | Signal      | Pin | Signal      | Pin |
|-------------|-----|-------------|-----|-------------|-----|
| DVDD (1.5V) | E11 | DVDD (1.5V) | J8  | DVDD (1.5V) | L9  |
| DVDD (1.5V) | E12 | DVDD (1.5V) | J9  | DVDD (1.5V) | L10 |
| DVDD (1.5V) | G5  | DVDD (1.5V) | J10 | VDDO (3.3V) | A3  |
| DVDD (1.5V) | G6  | DVDD (1.5V) | J11 | VDDO (3.3V) | A7  |
| DVDD (1.5V) | G13 | DVDD (1.5V) | K5  | VDDO (3.3V) | A11 |
| DVDD (1.5V) | H5  | DVDD (1.5V) | K6  | VDDO (3.3V) | E1  |
| DVDD (1.5V) | H6  | DVDD (1.5V) | K7  | VDDO (3.3V) | K3  |
| DVDD (1.5V) | H7  | DVDD (1.5V) | K8  | VDDO (3.3V) | K4  |
| DVDD (1.5V) | H8  | DVDD (1.5V) | K9  | VDDO (3.3V) | K13 |
| DVDD (1.5V) | H11 | DVDD (1.5V) | K10 | VDDO (3.3V) | N6  |
| DVDD (1.5V) | J5  | DVDD (1.5V) | K11 | VDDO (3.3V) | N8  |
| DVDD (1.5V) | J6  | DVDD (1.5V) | L4  | VDDO (3.3V) | P2  |
| DVDD (1.5V) | J7  | DVDD (1.5V) | L5  | VDDO (3.3V) | P12 |

Table 34. Analog Power Signals

| Signal        | Pin | Signal        | Pin | Signal        | Pin |
|---------------|-----|---------------|-----|---------------|-----|
| AVDDL (2.5 V) | D9  | AVDDL (2.5 V) | G12 | AVDDL (2.5 V) | L8  |
| AVDDL (2.5 V) | D11 |               |     |               |     |

**Table 35. Grounds and No Connect Signals**

| Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin |
|--------|-----|--------|-----|--------|-----|--------|-----|
| VSS    | B3  | VSS    | E7  | VSS    | G9  | NC     | A1  |
| VSS    | B7  | VSS    | E8  | VSS    | G10 | NC     | A14 |
| VSS    | C10 | VSS    | E9  | VSS    | G11 | NC     | C5  |
| VSS    | C12 | VSS    | E10 | VSS    | G14 | NC     | D10 |
| VSS    | D4  | VSS    | F4  | VSS    | H9  | NC     | D12 |
| VSS    | D5  | VSS    | F5  | VSS    | H10 | NC     | D14 |
| VSS    | D6  | VSS    | F6  | VSS    | K2  | NC     | F12 |
| VSS    | D7  | VSS    | F7  | VSS    | K12 | NC     | H12 |
| VSS    | D8  | VSS    | F8  | VSS    | L6  | NC     | J4  |
| VSS    | D13 | VSS    | F9  | VSS    | L11 | NC     | J13 |
| VSS    | E2  | VSS    | F10 | VSS    | M6  | NC     | L7  |
| VSS    | E4  | VSS    | F11 | VSS    | N1  | NC     | N11 |
| VSS    | E5  | VSS    | G7  | VSS    | N12 | NC     | P1  |
| VSS    | E6  | VSS    | G8  | VSS    | P8  | NC     | P14 |

**Table 36. Signal Names in Pin Order (Sheet 1 of 6)**

| Signal Name  | Pin |
|--------------|-----|
| NC           | A1  |
| SERR#        | A2  |
| 3.3V         | A3  |
| IDSEL        | A4  |
| AD[25]       | A5  |
| PME#         | A6  |
| 3.3V         | A7  |
| AD[30]       | A8  |
| LAN_PWR_GOOD | A9  |
| SMBCLK       | A10 |
| 3.3V         | A11 |
| LINK_UP#     | A12 |
| TEST         | A13 |
| NC           | A14 |
| AD[22]       | B1  |
| AD[23]       | B2  |
| VSS          | B3  |
| AD[24]       | B4  |

Table 36. Signal Names in Pin Order (Sheet 2 of 6) (Continued)

| Signal Name                 | Pin |
|-----------------------------|-----|
| AD[26]                      | B5  |
| AD[27]                      | B6  |
| VSS                         | B7  |
| AD[31]                      | B8  |
| RST#                        | B9  |
| SMB_ALERT#                  | B10 |
| LINK100#                    | B11 |
| LINK1000#                   | B12 |
| CTRL25                      | B13 |
| PHY REF                     | B14 |
| AD[21]                      | C1  |
| M66EN                       | C2  |
| REQ#                        | C3  |
| C/BE#[3]                    | C4  |
| NC                          | C5  |
| AD[28]                      | C6  |
| AD[29]                      | C7  |
| CLK_RUN#                    | C8  |
| SMBDATA                     | C9  |
| VSS                         | C10 |
| ACTIVITY#                   | C11 |
| VSS                         | C12 |
| MDI[0]+                     | C13 |
| MDI[0]-                     | C14 |
| AD[18]                      | D1  |
| AD[19]                      | D2  |
| AD[20]                      | D3  |
| ALT_CLK125 (connect to VSS) | D4  |
| VSS                         | D5  |
| VSS                         | D6  |
| VSS                         | D7  |
| VSS                         | D8  |
| 2.5 V                       | D9  |
| NC                          | D10 |
| 2.5 V                       | D11 |
| NC                          | D12 |
| VSS                         | D13 |
| NC                          | D14 |



**Table 36. Signal Names in Pin Order (Sheet 3 of 6) (Continued)**

| Signal Name                | Pin |
|----------------------------|-----|
| 3.3V                       | E1  |
| VSS                        | E2  |
| AD[17]                     | E3  |
| VSS                        | E4  |
| VSS                        | E5  |
| VSS                        | E6  |
| VSS                        | E7  |
| VSS                        | E8  |
| VSS                        | E9  |
| VSS                        | E10 |
| 1.5V                       | E11 |
| 1.5V                       | E12 |
| MDI[1]+                    | E13 |
| MDI[1]-                    | E14 |
| IRDY#                      | F1  |
| FRAME#                     | F2  |
| C/BE#[2]                   | F3  |
| VSS                        | F4  |
| VSS                        | F5  |
| VSS                        | F6  |
| VSS                        | F7  |
| VSS                        | F8  |
| VSS                        | F9  |
| VSS                        | F10 |
| VSS                        | F11 |
| PHY_TSTPT (do not connect) | F12 |
| MDI[2]+                    | F13 |
| MDI[2]-                    | F14 |
| CLK                        | G1  |
| VIO                        | G2  |
| TRDY#                      | G3  |
| ZP_COMP                    | G4  |
| 1.5V                       | G5  |
| 1.5V                       | G6  |
| VSS                        | G7  |
| VSS                        | G8  |
| VSS                        | G9  |
| VSS                        | G10 |

Table 36. Signal Names in Pin Order (Sheet 4 of 6) (Continued)

| Signal Name             | Pin |
|-------------------------|-----|
| VSS                     | G11 |
| 2.5 V                   | G12 |
| 1.5V                    | G13 |
| VSS                     | G14 |
| STOP#                   | H1  |
| INTA#                   | H2  |
| DEVSEL#                 | H3  |
| ZN_COMP                 | H4  |
| 1.5V                    | H5  |
| 1.5V                    | H6  |
| 1.5V                    | H7  |
| 1.5V                    | H8  |
| VSS                     | H9  |
| VSS                     | H10 |
| 1.5V                    | H11 |
| HSDACN (do not connect) | H12 |
| MDI3 +                  | H13 |
| MDI3 -                  | H14 |
| PAR                     | J1  |
| PERR#                   | J2  |
| GNT#                    | J3  |
| NC                      | J4  |
| 1.5V                    | J5  |
| 1.5V                    | J6  |
| 1.5V                    | J7  |
| 1.5V                    | J8  |
| 1.5V                    | J9  |
| 1.5V                    | J10 |
| 1.5V                    | J11 |
| AUX_PWR                 | J12 |
| HSDACP (do not connect) | J13 |
| XTAL2                   | J14 |
| AD[16]                  | K1  |
| VSS                     | K2  |
| 3.3V                    | K3  |
| 3.3V                    | K4  |
| 1.5V                    | K5  |
| 1.5V                    | K6  |

**Table 36. Signal Names in Pin Order (Sheet 5 of 6) (Continued)**

| Signal Name               | Pin |
|---------------------------|-----|
| 1.5V                      | K7  |
| 1.5V                      | K8  |
| 1.5V                      | K9  |
| 1.5V                      | K10 |
| 1.5V                      | K11 |
| AVSS                      | K12 |
| 3.3V                      | K13 |
| XTAL1                     | K14 |
| AD[14]                    | L1  |
| AD[15]                    | L2  |
| C/BE#[1]                  | L3  |
| 1.5V                      | L4  |
| 1.5V                      | L5  |
| VSS                       | L6  |
| CLK_BYP# (do not connect) | L7  |
| 2.5 V                     | L8  |
| 1.5V                      | L9  |
| 1.5V                      | L10 |
| VSS                       | L11 |
| JTAG_TMS                  | L12 |
| JTAG_RST#                 | L13 |
| JTAG_TCK                  | L14 |
| AD[11]                    | M1  |
| AD[12]                    | M2  |
| AD[13]                    | M3  |
| C/BE#[0]                  | M4  |
| AD[5]                     | M5  |
| VSS                       | M6  |
| AD[1]                     | M7  |
| CLK_VIEW                  | M8  |
| FL_CE#                    | M9  |
| EESK                      | M10 |
| FL_SI                     | M11 |
| SDP[7]                    | M12 |
| JTAG_TDI                  | M13 |
| JTAG_TDO                  | M14 |
| VSS                       | N1  |
| AD[10]                    | N2  |

Table 36. Signal Names in Pin Order (Sheet 6 of 6) (Continued)

| Signal Name | Pin |
|-------------|-----|
| AD[9]       | N3  |
| AD[7]       | N4  |
| AD[4]       | N5  |
| 3.3V        | N6  |
| AD[0]       | N7  |
| 3.3V        | N8  |
| FL_SCK      | N9  |
| EEDO        | N10 |
| NC          | N11 |
| VSS         | N12 |
| SDP[6]      | N13 |
| SDP[0]      | N14 |
| NC          | P1  |
| 3.3V        | P2  |
| AD[8]       | P3  |
| AD[6]       | P4  |
| AD[3]       | P5  |
| AD[2]       | P6  |
| EECS        | P7  |
| GND         | P8  |
| FLSH_SO     | P9  |
| EEDI        | P10 |
| CTRL15      | P11 |
| 3.3V        | P12 |
| SDP[1]      | P13 |
| NC          | P14 |

## 5.5 Visual Pin Reference

|    | A            | B          | C         | D          | E       | F         | G       | H       | J       | K      | L          | M        | N        | P       |
|----|--------------|------------|-----------|------------|---------|-----------|---------|---------|---------|--------|------------|----------|----------|---------|
| 1  | NC           | AD[22]     | AD[21]    | AD[18]     | 3.3V    | IRDY#     | CLK     | STOP#   | PAR     | AD[16] | AD[14]     | AD[11]   | VSS      | NC      |
| 2  | SERR#        | AD[23]     | M66EN     | AD[19]     | VSS     | FRAME#    | VIO     | INTA#   | PERR#   | VSS    | AD[15]     | AD[12]   | AD[10]   | 3.3V    |
| 3  | 3.3V         | VSS        | REQ#      | AD[20]     | AD[17]  | C/BE#[2]  | TRDY#   | DVSEL#  | GNT#    | 3.3V   | C/B3#[1]   | AD[13]   | AD[9]    | AD[8]   |
| 4  | IDSEL        | AD[24]     | C/BE#[3]  | ALT_CLK125 | VSS     | VSS       | ZP_COMP | ZN_COMP | NC      | 3.3V   | 1.5V       | C/BE#[0] | AD[7]    | AD[6]   |
| 5  | AD[25]       | AD[26]     | NC        | VSS        | VSS     | VSS       | 1.5V    | 1.5V    | 1.5V    | 1.5V   | 1.5V       | AD[5]    | AD[4]    | AD[3]   |
| 6  | PME#         | AD[27]     | AD[28]    | VSS        | VSS     | VSS       | 1.5V    | 1.5V    | 1.5V    | 1.5V   | VSS        | VSS      | 3.3V     | AD[2]   |
| 7  | 3.3V         | VSS        | AD[29]    | VSS        | VSS     | VSS       | VSS     | 1.5V    | 1.5V    | 1.5V   | CLK_BYP#   | AD[1]    | AD[0]    | EECS    |
| 8  | AD[30]       | AD[31]     | CLK_RUN#  | VSS        | VSS     | VSS       | VSS     | 1.5V    | 1.5V    | 1.5V   | 2.5V       | CLK_VIEW | 3.3V     | VSS     |
| 9  | LAN_PWR_GOOD | RST#       | SMBDATA   | 2.5V       | VSS     | VSS       | VSS     | VSS     | 1.5V    | 1.5V   | 1.5V       | FLSH_CE# | FLSH_SCK | FLSH_SO |
| 10 | SMBCLK       | SMB_ALERT# | VSS       | NC         | VSS     | VSS       | VSS     | VSS     | 1.5V    | 1.5V   | 1.5V       | EESK     | EEDO     | EEDI    |
| 11 | 3.3V         | LINK100#   | ACTIVITY# | 2.5V       | 1.5V    | VSS       | VSS     | 1.5V    | 1.5V    | 1.5V   | VSS        | FLSH_SI  | NC       | CTRL15  |
| 12 | LINK_UP#     | LINK1000#  | VSS       | NC         | 1.5V    | PHY_TSTPT | 2.5V    | HSDACN  | AUX_PWR | VSS    | JTAG_TMS   | SDP[7]   | VSS      | 3.3V    |
| 13 | TEST         | CTRL25     | MDI[0]+   | VSS        | MDI[1]+ | MDI[2]+   | 2.5V    | MDI[3]+ | HSDACP  | 3.3V   | JTAG_TRST# | JTAG_TDI | SDP[6]   | SDP[1]  |
| 14 | NC           | PHY REF    | MDI[0]-   | NC         | MDI[1]+ | MDI[2]+   | VSS     | MDI[3]+ | XTAL2   | XTAL1  | JTAG_TCK   | JTAG_TDO | SDP[0]   | NC      |

**Figure 12. Ball Grid Array / Pin Reference for 196-TFBGA (Bottom/Pin View)**

*Note:* Figure 12 is rotated 90 degrees counter-clockwise from the pin 1 position (corner) in Figure 11.



*Note:* This page is intentionally left blank.